Notice of Allowability	Application No.	Applicant(s)	
	10/626,228	SMITH ET AL.	
	Examiner	Art Unit	
	YOUNG T. TSE	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the amendment filed 09 May 2007*.

2. ☒ The allowed claim(s) is/are *1-6,8-15 and 17-23*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

1. The drawings were received on May 09, 2007. These drawings are acceptable.

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

The application has been amended as follows:

In claim 8, line 1, "claim 1" has been changed to "claim 6" in order to avoid the antecedent basis of said second circuit (see lines 1-2 of claim 6).

In claim 18, line 1, "a-first circuit" has been changed to "a first circuit" as listed in the original claim 18.

3. The following is an examiner's statement of reasons for allowance: the prior art fails to show or suggest that a method and repeater device for repeating source synchronous data comprising receiving the source synchronous data comprising a first data signal and a first clock signal, utilizing a reference clock signal and the first clock signal to generate a second clock signal, utilizing the second clock signal to latch first data signal, generating a third clock signal, and utilizing the third clock signal to transmit in a source synchronous manner a data signal and a clock signal corresponding to the first data and the first clock signal.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to YOUNG T. TSE whose telephone number is (571) 272-3051. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on (571) 272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

YOUNG T. TSE
Primary Examiner
Art Unit 2611

receive said reference clock signal; and

generate said second clock signal to be approximately ninety degrees out of phase with said first clock signal.

4. (Original) The device of claim 3, wherein the first circuit is selected from the group consisting of: a delay locked loop, and a phase locked loop.

5. (Original) The device of claim 3, wherein said first circuit is further configured to:

generate a fourth clock signal approximately ninety degrees out of phase with said first clock signal; and

shift the phase of said generated second clock signal a first number of degrees to be approximately ninety degrees out of phase with said first data signal.

6. (Currently Amended) The device of claim 5, further comprising a second circuit configured to:

receive said reference clock signal;

receive said fourth clock signal; and

generate ~~a fifth~~ said third clock signal to be approximately in phase with said fourth clock signal.

7. (Cancelled).

8. (Currently Amended) The device of claim ~~7~~ 6, wherein said second circuit is selected from the group consisting of: a delay locked loop, and a phase locked loop.

9. (Original) The device of claim 5, wherein the first circuit is trainable to determine said first number of degrees.

shifting the phase of said generated second clock signal a first number of degrees to be approximately ninety degrees out of phase with said first data signal.

15. (Currently Amended) The method of claim 14, further comprising:

receiving said reference clock signal in a second circuit;

receiving said fourth clock signal in the second circuit; and

generating ~~a fifth~~ said third clock signal to be approximately in phase with said fourth clock signal.

16. (Cancelled).

17. (Original) The method of claim 15, wherein said second circuit is selected from the group consisting of: a delay locked loop, and a phase locked loop.

18. (Original) The method of claim 14, further comprising training ~~a first~~ a first circuit which generates said second clock signal to determine said first number of degrees.

19. (Currently Amended) A source synchronous system comprising:

a source device configured to convey source synchronous data comprising a first data signal and a ~~corresponding~~ first clock signal;

a repeater device coupled to said source device, wherein said repeater device comprises:

a first interface configured to receive said source synchronous data;

a second interface configured to transmit source synchronous data; and

circuitry coupled to said first interface, wherein said circuitry is configured to:

utilize a reference clock signal and said first clock signal to generate a second clock signal;

utilize said second clock signal to latch said first data signal;

generate a third clock signal; and